Amendments to the Claims

Please cancel Claims 6, 17 and 24. Please amend claims 1, 3-5, 7, 11-16, 18, 19, and 21-23. The claim set below will replace all previous versions of the claims:

Claim Listing

1. (Currently amended) A data demultiplexer for demultiplexing data from a communication link, the data demultiplexer comprising:

~~a clock source;~~

a higher frequency data demultiplexer which demultiplexes the data on the communication link to an intermediate frequency signal in response to a first timing signal, ~~a clock signal from the clock source being precisely distributed to the higher frequency data demultiplexer~~;

a timing signal generator to generate a second timing signal in response to the first timing signal, wherein the second timing signal exhibits one pulse for every N pulses of the first timing signal, N being an integer value; and

a lower frequency data demultiplexer coupled to the higher frequency demultiplexer which ~~further~~ demultiplexes the intermediate frequency signal to a demultiplexed data signal in response to the second timing signal;

wherein a maximum timing error of the second timing signal tolerable by the lower frequency demultiplexer substantially exceeds a maximum timing error of the first timing signal tolerable by the higher frequency demultiplexer, ~~the clock signal being less precisely distributed to the lower frequency data demultiplexer~~.

2. (Previously presented) A data demultiplexer as claimed in claim 1 wherein the higher frequency data demultiplexer and the lower frequency data demultiplexer are formed on a single circuit chip.

3. (Currently amended) A data demultiplexer as claimed in claim [[2]] 1 wherein the timing signal generator comprises circuitry to frequency-divide the first timing signal to generate

the second timing signal ~~the clock signal is frequency divided to clock the lower frequency data demultiplexor~~.

4. (Currently amended) A data demultiplexer as claimed in claim 3 wherein the circuitry to frequency-divide the first timing signal comprises ~~clock signal is frequency divided by~~ a ~~ring~~ counter.

5. (Currently amended) A data demultiplexer as claimed in claim [[1]] 4 wherein the counter comprises a ring counter~~clock signal is frequency divided to clock the lower frequency data demultiplexor~~.

6. (Cancelled)

7. (Currently amended) A data demultiplexer as claimed in claim 1 further comprising a multiplying delay locked loop bit clock generator to generate the first timing signal ~~in which the higher frequency data multiplexer is clocked by a multiplying delay locked loop bit clock generator~~.

8. (Original) A data demultiplexer as claimed in claim 1 wherein the data on the communication link comprises a one-bit-wide bitstream.

9. (Original) A data demultiplexer as claimed in claim 8 wherein the intermediate frequency signal is two bits wide.

10. (Original) A data demultiplexer as claimed in claim 1 wherein the intermediate frequency signal comprises more than two parallel bits.

11. (Currently amended) A data demultiplexer as claimed in claim 10 wherein the first timing signal comprises ~~higher frequency data multiplexer is clocked by~~ an N-phase overlapping clock.

12. (Currently amended) A method of demultiplexing data from a communication link comprising:

demultiplexing the data from the communication link to an intermediate frequency signal in response to a first timing signal~~using a clock signal precisely distributed from a clock source~~;

generating a second timing signal in response to the first timing signal, wherein the second timing signal exhibits one pulse for every N pulses of the first timing signal, N being an integer value; and

~~further~~ demultiplexing the intermediate frequency signal to a lower frequency signal ~~using the clock signal less precisely distributed from the clock source~~in response to the second timing signal, wherein a maximum tolerable timing error of the second timing signal substantially exceeds a maximum tolerable timing error of the first timing signal.

13. (Currently amended) A method of demultiplexing as claimed in claim 12 wherein demultiplexing the data from the communication link ~~the steps are performed in~~ comprises demultiplexing the data within a higher frequency data demultiplexing stage and demultiplexing the intermediate frequency signal comprises demultiplexing the intermediate frequency signal within ~~and~~ a lower frequency data demultiplexing stage, the higher frequency data demultiplexing stage and lower frequency data demultiplexing stage being formed on a single circuit chip.

14. (Currently amended) A method of demultiplexing as claimed in claim [[13]] 12 wherein [[the]] generating a second timing signal in response to the first timing signal comprises frequency-dividing the first timing signal~~clock signal is frequency divided to clock the lower frequency data multiplexing stage~~.

15. (Currently amended) A method of demultiplexing as claimed in claim 14 wherein ~~the clock~~ frequency-dividing the first timing signal comprises frequency-dividing the first timing signal in a counter~~is frequency divided by a ring counter~~.

16. (Currently amended) A method of demultiplexing as claimed in claim [[12]] 14 wherein frequency-dividing the first timing signal in a counter comprises frequency-dividing the first timing signal in a ring counter~~the clock signal is frequency-divided to clock the lower frequency data multiplexing stage~~.

17. (Cancelled)

18. (Currently amended) A method of demultiplexing as claimed in claim 12 further comprising generating the first timing signal within ~~in which the higher frequency data multiplexer is clocked by~~ a multiplying delay locked loop bit clock generator.

19. (Currently amended) A method of demultiplexing as claimed in claim 12 wherein the data from ~~higher frequency signal on~~ the communication link comprises a one-bit-wide bitstream.

20. (Original) A method of demultiplexing as claimed in claim 19 wherein the intermediate frequency signal is two bits wide.

21. (Currently amended) A method of demultiplexing as claimed in claim [[20]] 12 wherein the intermediate frequency signal comprises more than two parallel bits.

22. (Currently amended) A method of demultiplexing as claimed in claim 21 wherein the first timing signal comprises ~~higher frequency data multiplexer is clocked by~~ an N-phase overlapping clock.

23. (Currently amended) A data demultiplexer for demultiplexing data from a communication link comprising:

~~high frequency data demultiplexer~~ means ~~relying on a clock signal precisely distributed from a clock source~~ for demultiplexing the data on the communication link to an intermediate frequency signal in response to a first timing signal;

means for generating a second timing signal in response to the first timing signal, wherein the second timing signal exhibits one pulse for every N pulses of the first timing signal, N being an integer value; and

~~lower frequency data demultiplexer~~ means ~~relying on the clock signal less precisely distributed from the clock source~~ for demultiplexing the intermediate frequency signal to a lower frequency signal in response to the second timing signal, wherein a maximum tolerable timing error of the second timing signal substantially exceeds a maximum tolerable timing error of the first timing signal.

24. (Cancelled)